IR3621 EVALUATION BOARD USER GUIDE

Dual output using MOSFETs in SO8 package

INTRODUCTION

DESCRIPTION

The IR3621 IC combines a Dual synchronous Buck controller, providing a cost-effective, high performance and flexible solution. The IR3621 can be configured in 2-independent output or as a 2-phase mode. The 2-phase configuration is ideal for high current applications. The IR3621 features 180° out of phase operation which reduces the required input/output capacitance. Other key features offered by this device include two independent programmable soft starts, PreBias start up, programmable switching frequency up to 500KHz per phase, external frequency synchronization and under voltage lockout for proper start up. The current limit is provided by sensing the lower MOSFET's on-resistance for optimum cost and performance.

SPECIFICATION DATA

This reference board is designed for Dual output configuration and will demonstrate the main features of IC.
This user guide contains the schematic and bill of materials, the design guidelines are described in data sheet.

INPUT/OUTPUT CONNECTIONS

The following is the input/output connections:

Inputs:
JP1: Vin and Gnd
JU4: VCC and Gnd
JU5: VCL

Outputs:

JP2: Vout1
JP5: Vout2

Scope Probe connections:
J1 and J3: Inductor point for L2 and L3
J2 and J4: Outputs for Vout1 and Vout2

PGOOD: JU1

SYNC: JU2

The connection points for dual output application are shown in Figure 1. Connect the power supply cables according to this figure, minimizing wire lengths to reduce losses in the wire. Test points J1, J2, J3 and J4 provide easy connection for oscilloscope voltage probe to monitor the inductor points for each PWM section and output voltages.

Application Data:

V_{IN} = 12V
V_{OUT1} = 2.5V
I_{OUT1} = 10A
V_{OUT2} = 1.8V
I_{OUT2} = 10A
ΔV_{OUT} = 50mV
F_S = 400KHz

CONNECTION DIAGRAM

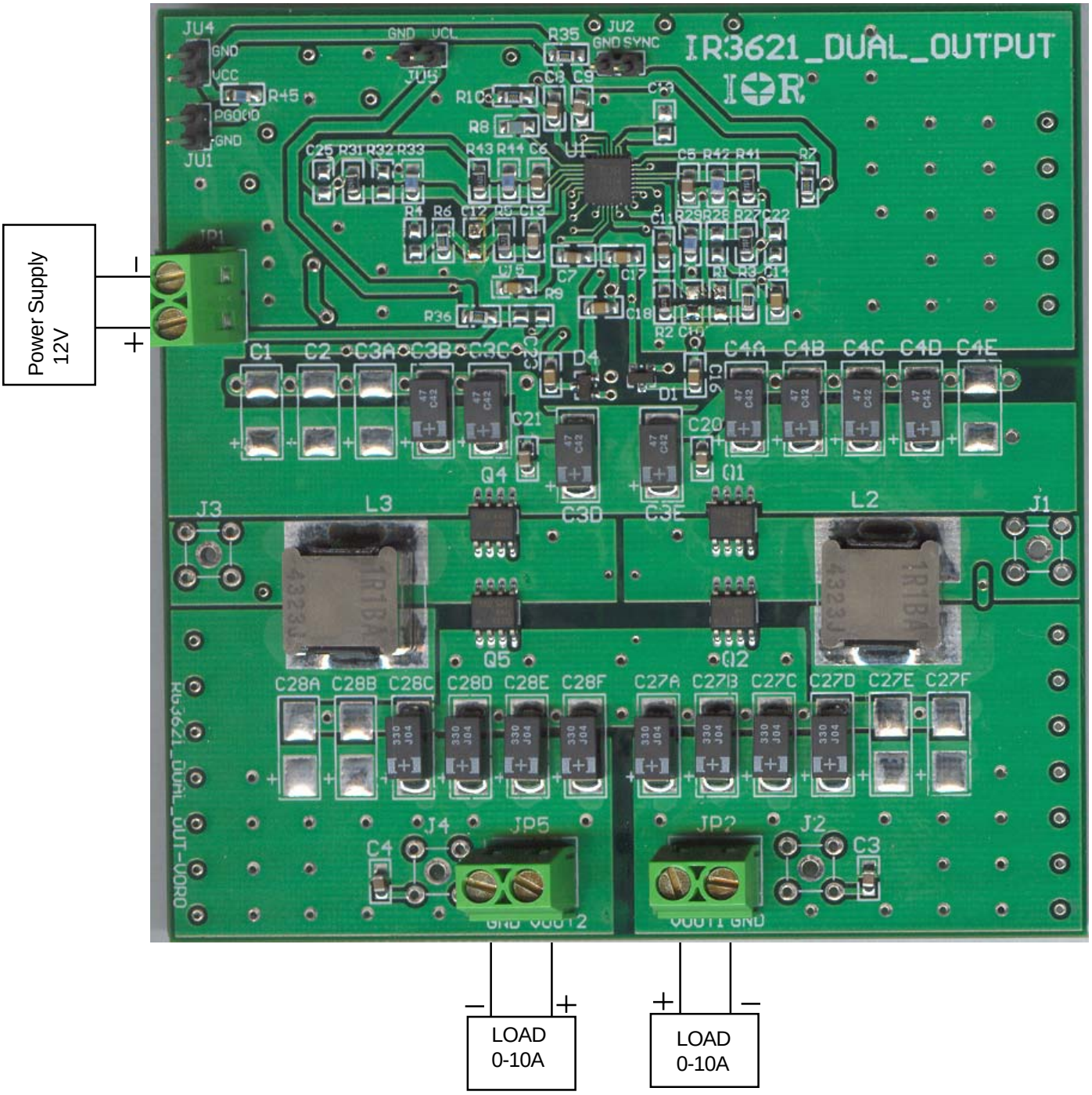

Figure 1 - Connection diagram of evaluation-board

LAYOUT

The PCB is 4-layers FR4 board, the top layer is dedicated for power components, with control MOSFETs and Synchronous MOSFETs. These MOSFETs are SOIC-8 footprint. The input capacitors are all located close to MOSFETs. The two output inductors are located closed to MOSFETs.

The two mid-layers are dedicated for Analog and Power ground, these two grounds are kept separated from each other and they are connected at a single point as shown in Figure3.

All the decoupling capacitors, charge pump capacitor and feedback components are located close to the IC. The feedback resistors are tied to the output voltage at the point of regulation and are located close to the IC.

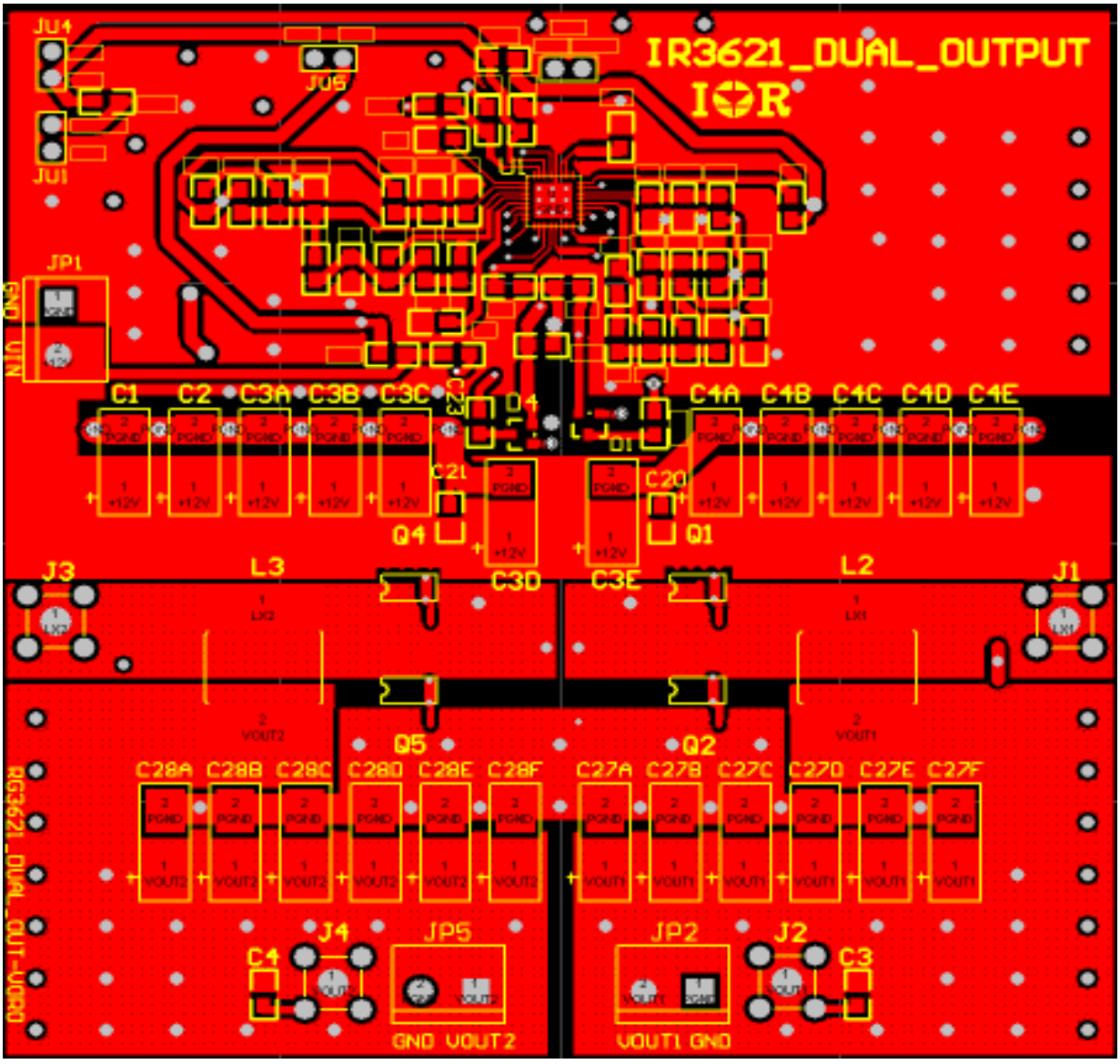

Figure 2 - Top layer of evaluation-board

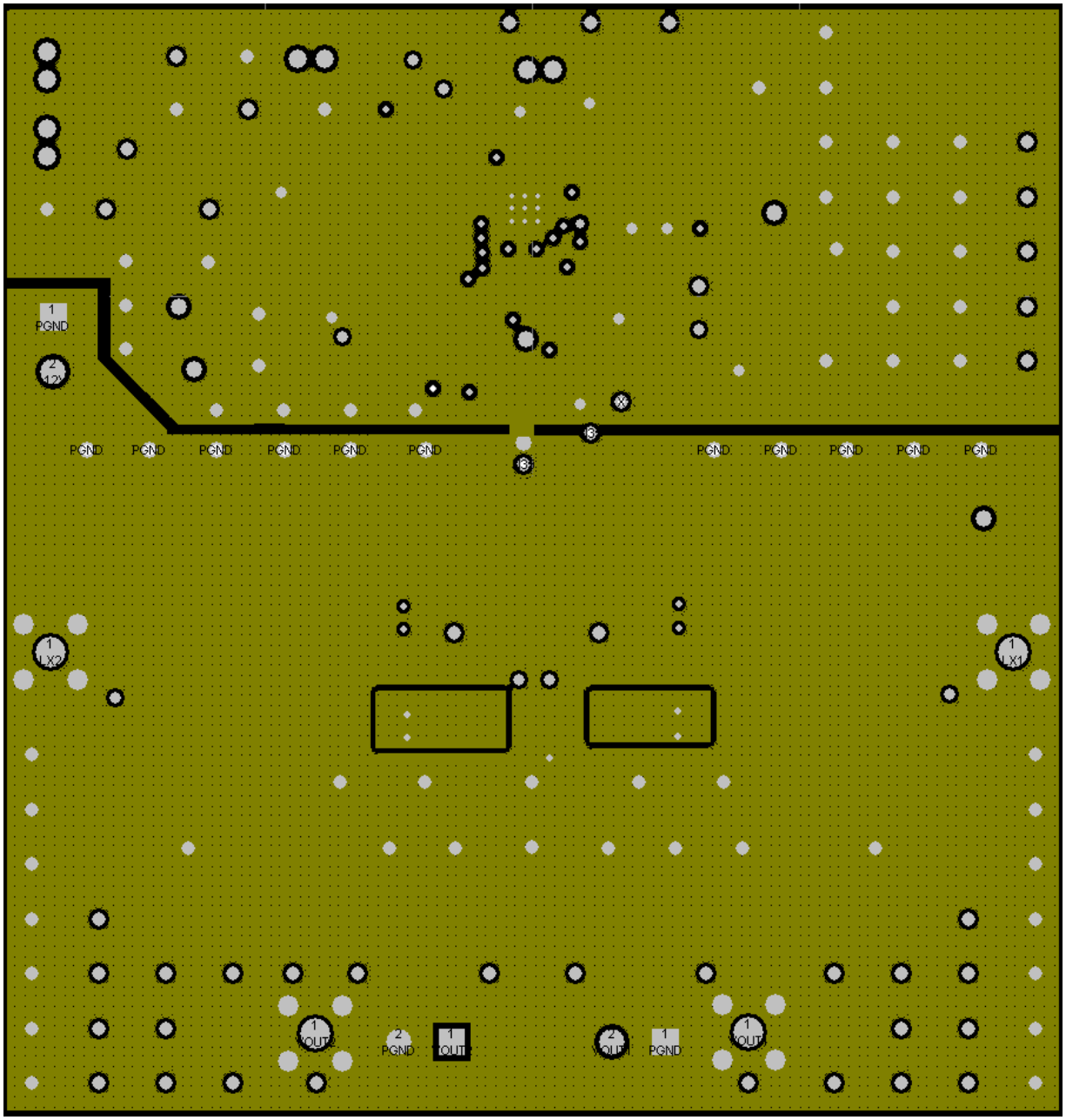

Figure 3 - Mid layer of evaluation-board

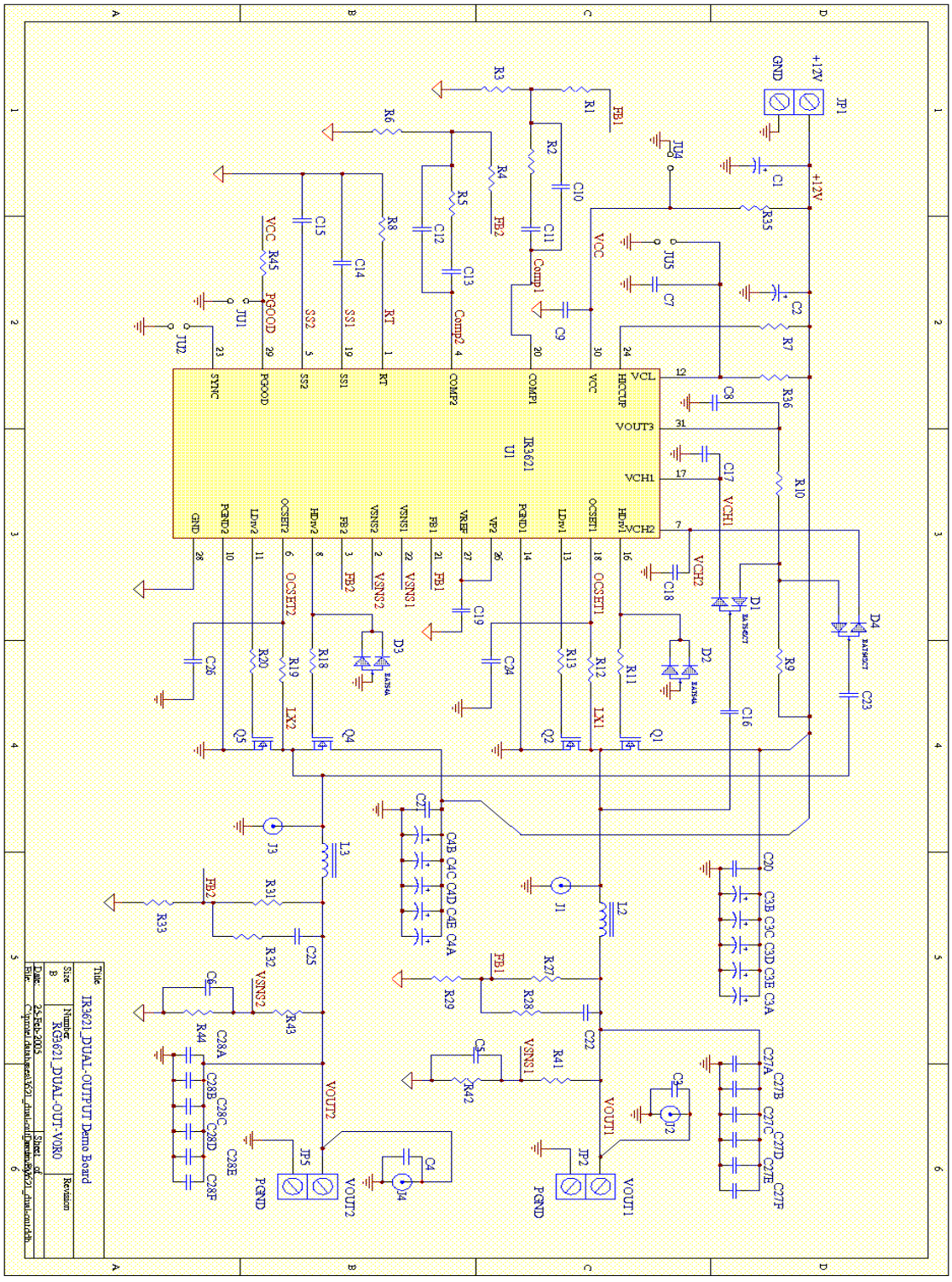

Figure 4 - Schematic of the evaluation Board

BILL OF MATERIAL For Dual Output Application, Vin=12V, Vout1=2.5V@10A, Vout2=1.8V@10A, Fs=400KHz

Ref Desig	Description	Value	Qty	Part#	Manuf
Q1,Q4	MOSFET	30V,11mOhm	2	IRF7821	IR
Q2,Q5	MOSFET	30V, 6mOhm	2	IRF8113	IR
U1	Controller	Synchronous PWM	1	IR3621M	IR
D1,D4	Diode	Fast Switching	2	BAT54S	IR
D2,D3	Diode	Fast Switching	2	BAT54A	IR
L2,L3	Inductor	1.1μH,16A	2	ETQP6F1R1BFA	Panasonic
C3B-D, C4A-E	Cap,Poscap	47μF, 16V,70mΩ	8	16TPB47M	Sanyo
C27A-D, C28C-F	Cap,Poscap	330μF,6.3V,40mΩ	8	6TPB330M	Sanyo
C14,C15,C16,C17,C18,C23	Cap,Ceramic	0.1μF, Y5V, 25V	6	ECJ-2VF1E104Z	Panasonic
C3,C4,C5,C6,C7,C8,C9,C20,C21	Cap,Ceramic	1μF, Y5V, 16V	9	ECJ-2VF1C105Z	Panasonic
C13	Cap,Ceramic	10nF, X7R, 50V	1	ECJ-2VB1H103K	Panasonic
C11	Cap,Ceramic	8.2nF,X7R,50V	1	ECJ-2VB1H822K	Panasonic
R2	Resistor	6.2K	1	Any	
R5	Resistor	4.7K	1		
R8	Resistor	22.6K	1		
R12,R19	Resistor	5.11K, 1%	2		
R27,R41	Resistor	2.15K, 1%	2		
R29,R33,R42,R44	Resistor	1K, 1%	4		
R31,R43	Resistor	1.24K,1%	2		
R45	Resistor	49.9K,1%	1		
R3,6,7,10,11,13,18,20,35,36	Resistor	Short, 0Ω	10		
R1,4,9,32,	Resistor	Open	4		
C1,2,C3A,C3E, C27E-F,C28A-B,	Capacitor	Open	8		
C10,12,19,22,24,25,26	Capacitor	Open	7		
J1,J2,J3,J4	Scope Probe		4	131-5031-00	Tektronix
JP1,JP2,JP5	Terminal	2-Pos terminal	3	ED1973-ND	Digi-Key
JU1,JU2,JU4,JU5	Jumper		4	S1012-02-ND	Digi-Key

TYPICAL OPERATING Waveforms

Test Conditions:
V_{IN}=12V, V_{OUT1}=2.5V, I_{OUT1}=0-10A, V_{OUT2}=1.8V, I_{OUT2}=0-10A, Fs=400KHz, T_A=Room Temp, No Air Flow Unless otherwise specified.

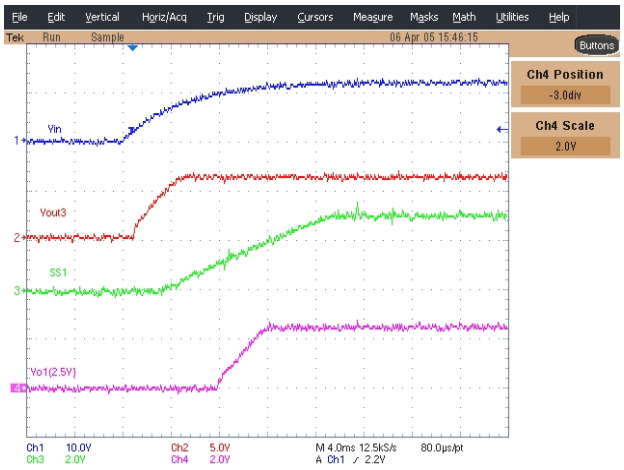

Figure 5 - Start up wavforms for 2.5V output
Ch1: Vin, Ch2: Vout3, Ch3: SS1, Ch4:Vo1 (2.5V)

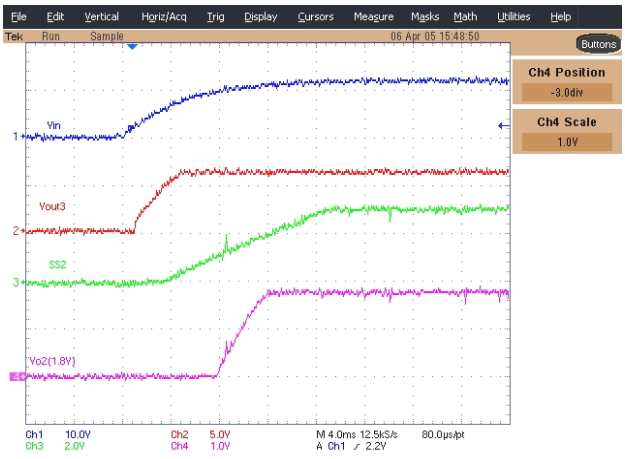

Figure 6 - Start up wavforms for 1.8V output
Ch1: Vin, Ch2: Vout3, Ch3: SS2, Ch4:Vo2 (1.8V)

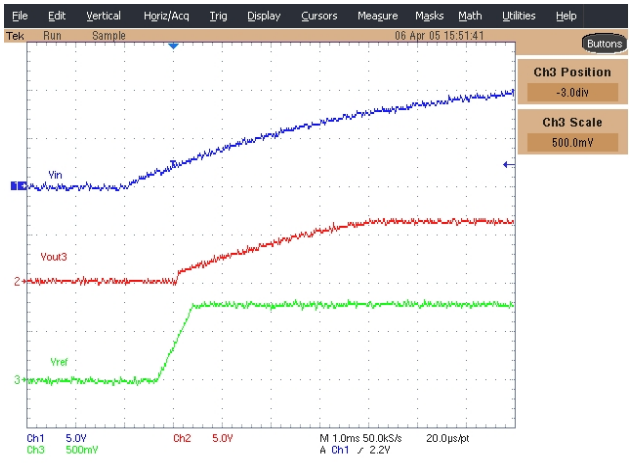

Figure 7 - Start up wavforms
Ch1: Vin, Ch2: Vout3, Ch3: Vref

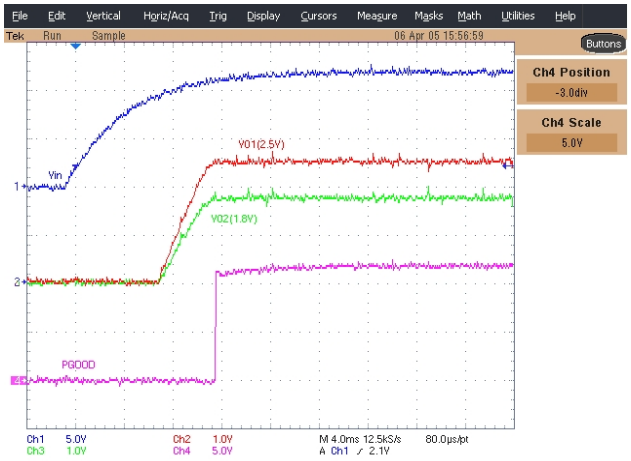

Figure 8 - Vo1, Vo2 and PGood
Ch1: Vin, Ch2: Vo1, Ch3: Vo2, Ch4: PGood

TYPICAL OPERATING Waveforms

Test Conditions:
V_{IN}=12V, V_{OUT1}=2.5V, I_{OUT1}=0-10A, V_{OUT2}=1.8V, I_{OUT2}=0-10A, Fs=400KHz, Ta=Room Temp, No Air Flow Unless otherwise specified.

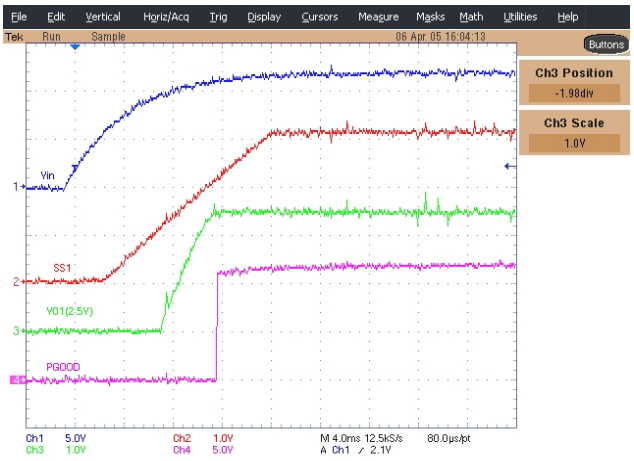

Figure 9 - 2.5V output
Ch1: Vin, Ch2: SS1, Ch3: Vo1, Ch4: PGood

Figure 10 - 1.8V output
Ch1: Vin, Ch2: SS2, Ch3: Vo2, Ch4: PGood

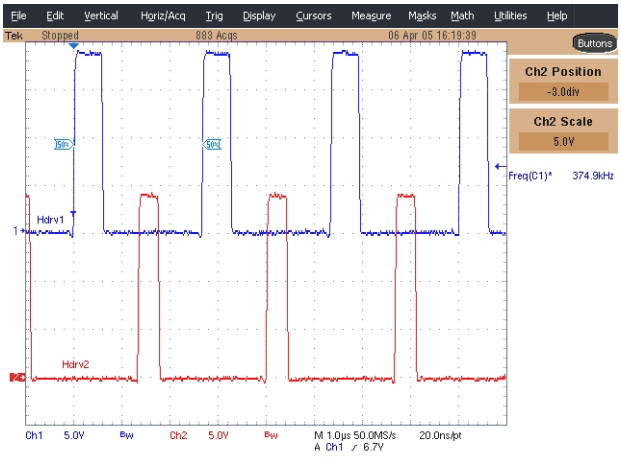

Figure11 - Gate waveforms with 180º out of phase
Ch1: Hdrv1, Ch2: Hdrv2

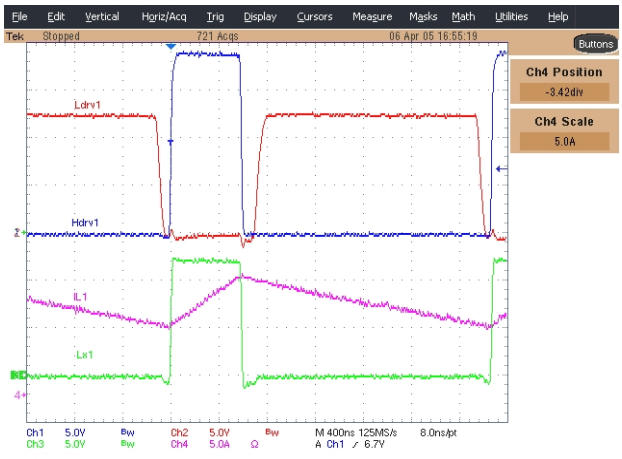

Figure 12 - 2.5V Waveforms
Ch1: Hdrv1, Ch2: Ldrv1, Ch3: Lx1, Ch4: Inductor Current

TYPICAL OPERATING Waveforms

Test Conditions:
V_{IN}=12V, V_{OUT1}=2.5V, I_{OUT1}=0-10A, V_{OUT2}=1.8V, I_{OUT2}=0-10A, Fs=400KHz, Ta=Room Temp, No Air Flow Unless otherwise specified.

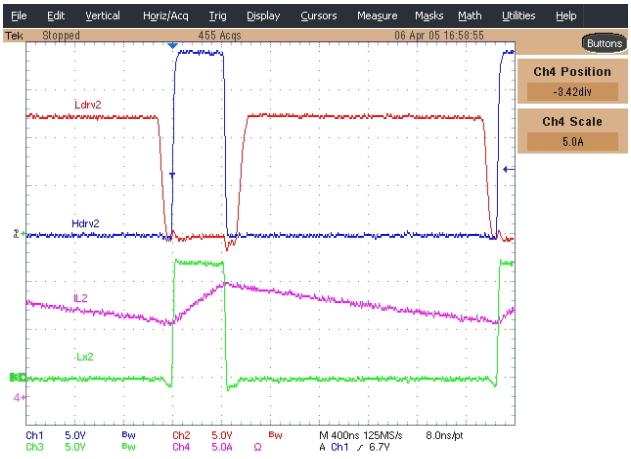

Figure 13 - 2.5V Waveforms
Ch1: Hdrv2, Ch2: Ldrv2, Ch3: Lx2, Ch4: Inductor Current

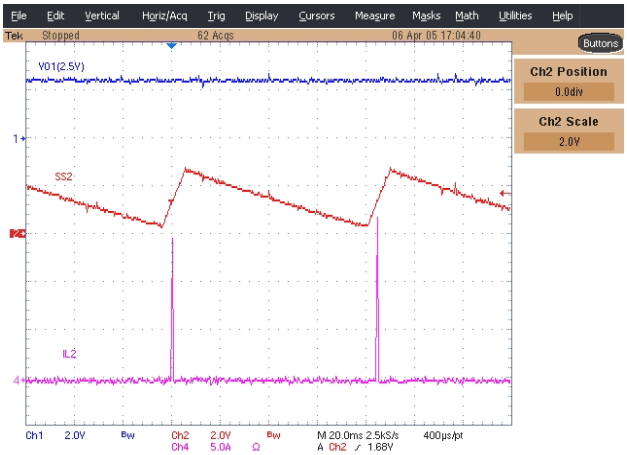

Figure14 - 1.8V output shorted
Ch1: Vo1, Ch2: SS2, Ch3: Inductor Current

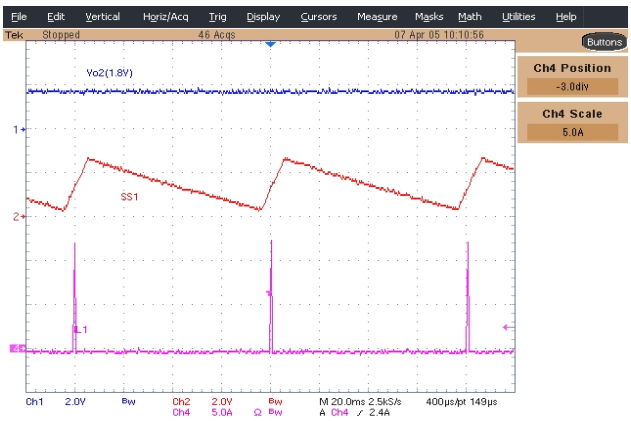

Figure 15 - 2.5V output shorted
Ch1: Vo2, Ch2: SS1, Ch3: Inductor Current

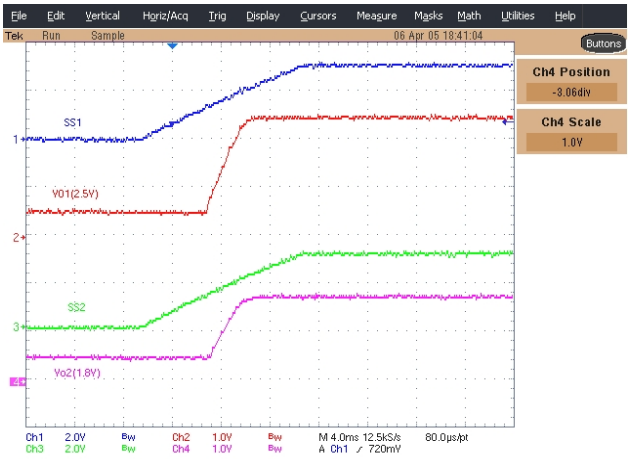

Figure 16 - Prebias Start up
Ch1: SS1, Ch2: Vo1, Ch3: SS2, Ch4:Vo2

TYPICAL OPERATING Waveforms

Test Conditions:
V_{IN}=12V, V_{OUT1}=2.5V, I_{OUT1}=0-10A, V_{OUT2}=1.8V, I_{OUT2}=0-10A, Fs=400KHz, Ta=Room Temp, No Air Flow Unless otherwise specified.

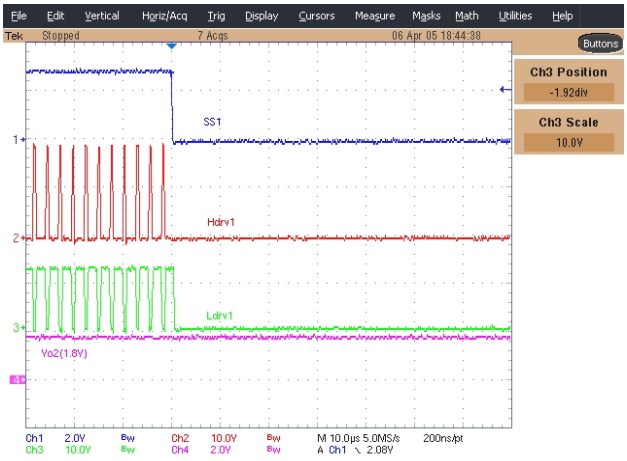

Figure 17 - SS1 pin shorted to Gnd
Ch1: SS1, Ch2: Hdrv1, Ch3: Ldrv1, Ch4:Vo2

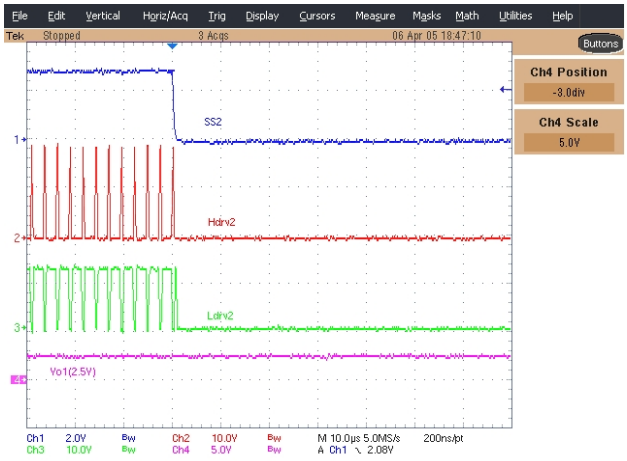

Figure 18 - SS2 pin shorted to Gnd
Ch1: SS2, Ch2: Hdrv2, Ch3: Ldrv2, Ch4:Vo1

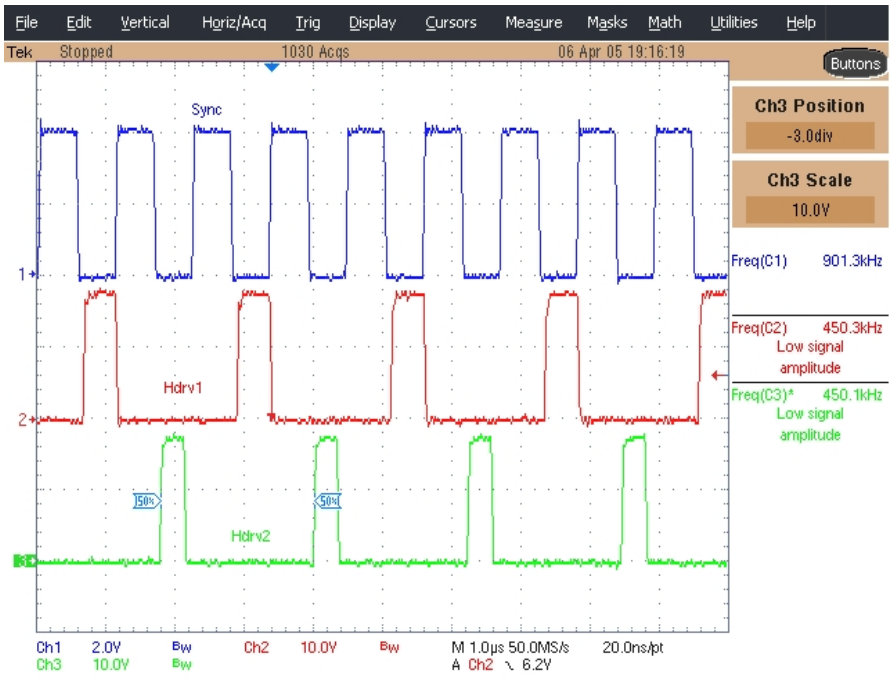

Figure 19 - Extrnal Synchronization
Ch1: Extrnal Clocl, Ch2: Hdrv1, Ch3: Hdrv2

TYPICAL OPERATING Waveforms

Test Conditions:
V_{IN}=12V, V_{OUT1}=2.5V, I_{OUT1}=0-10A, V_{OUT2}=1.8V, I_{OUT2}=0-10A, Fs=400KHz, Ta=Room Temp, No Air Flow Unless otherwise specified.

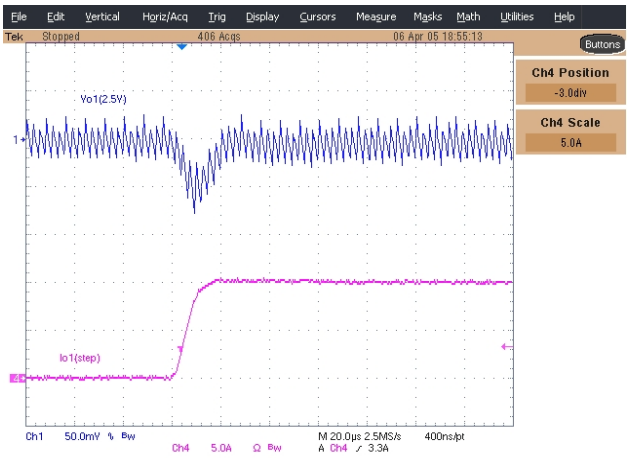

Figure 20 - Load Transient Respons for Vo1
(Io=0 to 10A)
Ch1: Vo1, Ch4: Io1

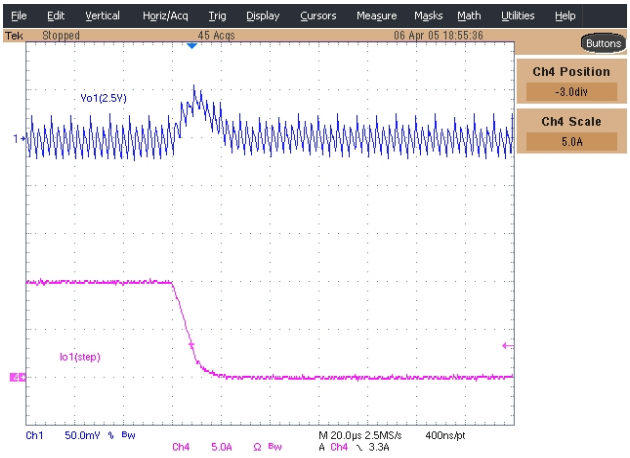

Figure 21 - Load Transient Respons for Vo1
(Io=10 to 0A)
Ch1: Vo1, Ch4: Io1

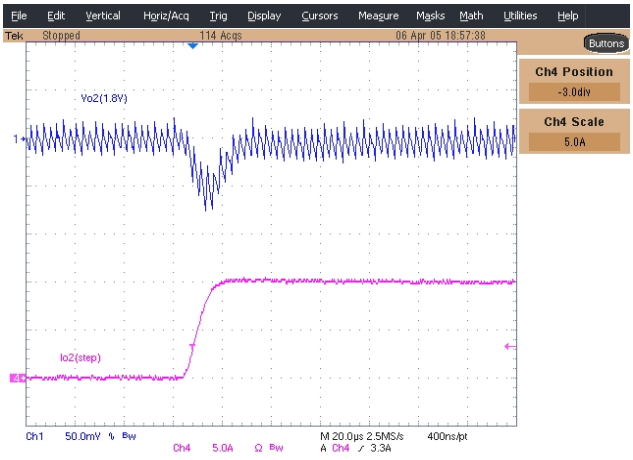

Figure 22 - Load Transient Respons for Vo2
(Io=0 to 10A)
Ch1: Vo2, Ch4: Io2

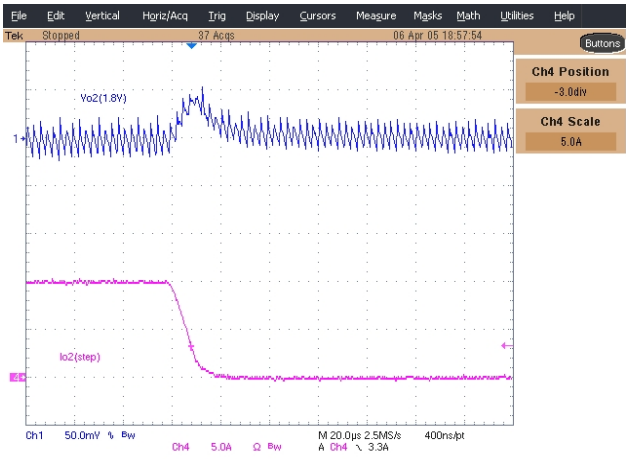

Figure 23 - Load Transient Respons for Vo2
(Io=10 to 0A)
Ch1: Vo2, Ch4: Io2

TYPICAL PERFORMANCE CURVES

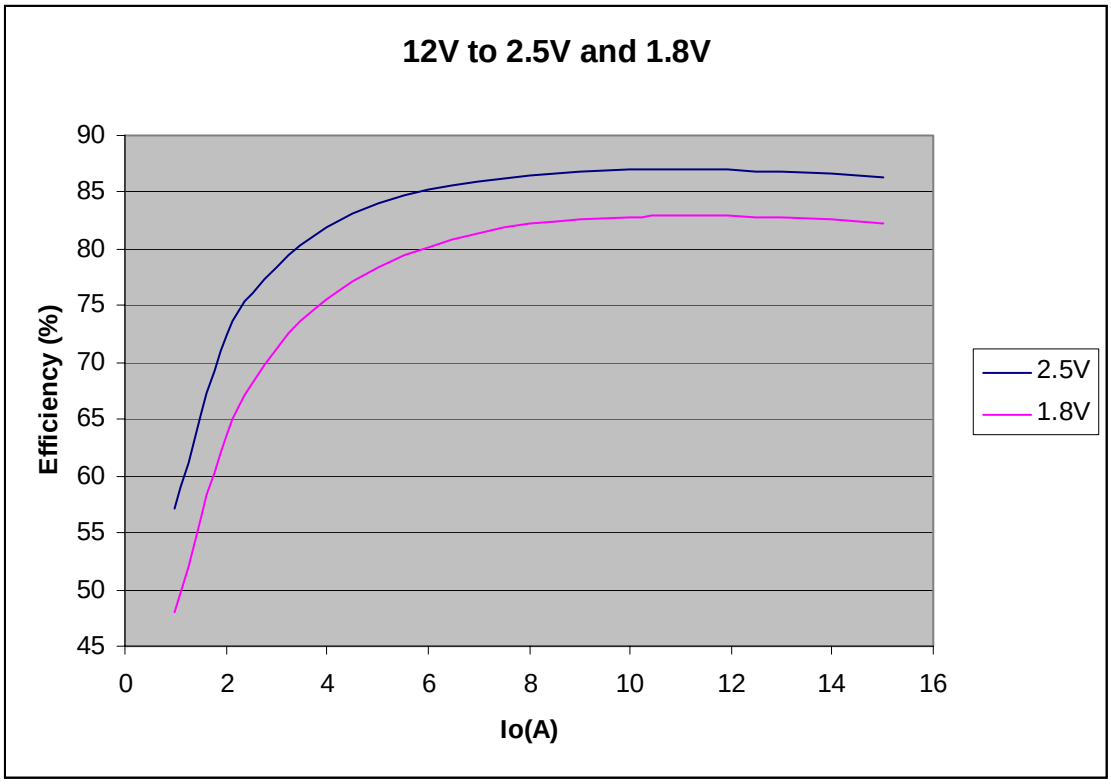

Figure 24- Efficiency for 2.5V and 1.8V outputs at room temperature no air flow. When measuring one output, the other output was running at no load.

Figure 25- Thermal Images for Both Outputs at Vin:12V, Vout1:2.5V @ 10A, Vout2:1.8V @ 10A. Room Temperature, No Air Flow

Test Point: 1) Sync FET for 2.5V output
2)Sync FET for 1.8V output
3) IR3621M IC.