

PIC18FXX2 Rev. C0 Silicon/Data Sheet Errata

The PIC18FXX2 Rev. C0 parts you have received conform functionally to the Device Data Sheet (DS39564B), except for the anomalies described below.

All the issues listed here will be addressed in future revisions of the PIC18FXX2 silicon.

The following silicon errata apply only to PIC18FXX2 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F242	00 0100 100	00111
PIC18F252	00 0100 000	00111
PIC18F442	00 0100 101	00111
PIC18F452	00 0100 001	00111

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFEh:3FFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: Core (Program Memory Space)

Performing table read operations above the user program memory space (addresses over 1FFFFh) may yield erroneous results at the extreme low end of the device's rated temperature range (-40°C).

This applies specifically to addresses above 1FFFFh, including the user ID locations (20000h-20007h), the configuration bytes (30000h-3000Dh) and the device ID locations (3FFFEh and 3FFFFh). User program memory is unaffected.

Work around

Three possible work arounds are presented. Other solutions may exist.

1. Do not perform table read operations on areas above the user memory space at -40°C.
2. Insert NOP instructions (specifically, literal FFFh) around any table read instructions. The suggested optimal number is 4 instructions before and 8 instructions after each table read. This may vary depending upon the particular application and should be optimized by the user.

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: Data EEPROM

When reading the data EEPROM, the contents of the EEDATA register may be corrupted if the RD bit (EECON1<0>) is set immediately following a write to the address byte (EEADR). The actual contents of the data EEPROM remain unaffected.

Work around

Do not set EEADR immediately before the execution of a read. Write to EEADR at least one instruction cycle before setting the RD bit. The instruction between the write to EEADR and the read can be any valid instruction, including a NOP.

Date Codes that pertain to this issue:

All engineering and production devices.

PIC18FXX2

3. Module: MSSP (All I²C™ and SPI™ Modes)

The Buffer Full (BF) flag bit of the SSPSTAT register (SSPSTAT<0>) may be inadvertently cleared even when the SSPBUF register has not been read. This will occur only when the following two conditions occur simultaneously:

- The four Least Significant bits of the BSR register are equal to 0Fh (BSR<3:0> = 1111) and
- Any instruction that contains C9h in its 8 Least Significant bits (i.e., register file addresses, literal data, address offsets, etc.) is executed.

Work around

All work arounds will involve setting the contents of BSR<3:0> to some value other than 0Fh.

In addition to those proposed below, other solutions may exist.

1. When developing or modifying code, keep these guidelines in mind:
 - Assign 12-bit addresses to all variables. This allows the assembler to know when access banking can be used.
 - Do not set the BSR to point to Bank 15 (BSR = 0Fh).
 - Allow the assembler to manipulate the access bit present in most instructions. Accessing the SFRs in Bank 15 will be done through the Access Bank. Continue to use the BSR to select all GPR Banks.
2. If accessing a part of Bank 15 is required and the use of access banking is not possible, consider using indirect addressing.
3. If pointing the BSR to Bank 15 is unavoidable, review the absolute file listing. Verify that no instructions contain C9h in the 8 Least Significant bits while the BSR points to Bank 15 (BSR = 0Fh).

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: Core (Instruction Set)

The Decimal Adjust W register instruction, DAW, may improperly clear the Carry bit (STATUS<0>) when executed.

Work around

Test the Carry bit state before executing the DAW instruction. If the Carry bit is set, increment the next higher byte to be added using an instruction such as INCF SZ (this instruction does not affect any Status flags and will not overflow a BCD nibble). After the DAW instruction has been executed, process the Carry bit normally (see Example 1).

EXAMPLE 1: PROCESSING THE CARRY BIT DURING BCD ADDITIONS

```
MOVLW 0x80      ; .80 (BCD)
ADDLW 0x80      ; .80 (BCD)

BTFSC STATUS,C  ; test C
INCFSZ byte2    ; inc next higher LSB
DAW

BTFSC STATUS,C  ; test C
INCFSZ byte2    ; inc next higher LSB

This is repeated for each DAW instruction.
```

5. Module: Reset

It has been observed that in certain Reset conditions, including power-up, the first GOTO instruction at address 0x0000 may not be executed. This occurrence is rare and affects very few applications.

To determine if your system is affected, test a statistically significant number of applications across the operating temperature, voltage and frequency ranges of the application. Affected systems will repeatably fail normal testing. Systems not affected will continue to not be affected over time.

Work around

Insert a NOP instruction at address 0x0000.

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: Program Memory

A very small number of applications are experiencing a low failure rate when using self-write through code types of applications. The most common of these are bootloader operations. This failure mechanism is characterized by a few bytes in program memory not being written as expected.

If this failure is going to occur, it will occur during a self-write operation. If a failure is not immediately observed, then there will be no data retention issues. The failure does not occur when using an external programmer through In-Circuit Serial Programming™ (ICSP™).

This failure mechanism is dependent on the sequence of instructions executed after self-writes. Good power supply decoupling minimizes this issue. It is recommended that you use a 0.1 μF decoupling capacitor with each power pin pair. The decoupling capacitor should be placed very close to the power pins.

It is recommended that you perform statistically significant testing within your application's operating range (i.e., temperature and voltage) with devices from multiple lots.

Work around

1. This work around only applies to PIC18F252 and PIC18F452 devices.

The program memory is divided into discrete panels and the failure has only been observed when a table write is executed from the same panel it is programming. The table write (self-write) within the same memory panel (0x0000 to 0x3FFF and 0x4000 to 0x7FFF) initiates a condition that can cause a failure. The firmware work around is to duplicate the partial bootloader (two instantiations of write functions) in two panels and ensure that the bootloader code always programs a different panel from where it resides. To accomplish this, do the following:

- Receive data from communication channel (normal operation for the bootloader).
- Identify address to be written.

- If writing to an address within the same memory panel that you are executing from (0x0000 to 0x3FFF and 0x4000 to 0x7FFF), then jump to the opposite memory panel. If the bootloader resides between location 0x0000 to 0x3FFF, and writing to an address between 0x0000 to 0x3FFF, then jump to another instantiation of the code located between 0x4000 to 0x7FFF and vice versa.
 - Always load holding latches (loading of `TABLAT` and then `TBLWT*`) from the opposite panel. This will require duplicate code in each panel to load data.
 - Always initiate write from the opposite panel. This will require duplicate code in each panel for the unlock sequence and setting up the write bit.
 - At the end of the successful write, code can return to the primary panel to get the next data.
2. Use a similar device from the PIC18F4520 family.

PIC18FXX2

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39564B), the following clarifications and corrections should be noted.

1. Module: DC Characteristics

The values for parameters, D005, D010A, D022A and D022B, shown in **Section 22.1 “DC Characteristics”** of the Device Data Sheet have changed (modified text is shown in **bold**):

22.1 DC Characteristics: PIC18FXX2 (Industrial, Extended) PIC18LFXX2 (Industrial)

PIC18LFXX2 (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial					
PIC18FXX2 (Industrial, Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended					
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
D005	VBOR	Brown-out Reset Voltage					
		PIC18LFXX2					
		BORV1:BORV0 = 11	1.96	2.06	2.16	V	$85^{\circ}\text{C} \geq T \geq 25^{\circ}\text{C}$
		BORV1:BORV0 = 10	2.64	2.78	2.92	V	
		BORV1:BORV0 = 01	4.11	4.33	4.55	V	
		BORV1:BORV0 = 00	4.41	4.64	4.87	V	
D005		PIC18FXX2					
		BORV1:BORV0 = 1x	N.A.	—	N.A.	V	Not in operating voltage range of device
		BORV1:BORV0 = 01	4.16	—	4.5	V	
		BORV1:BORV0 = 00	4.45	—	4.83	V	
D005		PIC18FXX2					
		BORV1:BORV0 = 1x	N.A.	—	N.A.	V	Extended devices operating at 125°C
		BORV1:BORV0 = 01	4.07	—	4.59	V	
		BORV1:BORV0 = 00	4.36	—	4.92	V	

Legend: Shading of rows is to assist in readability of the table.

Note 1: This is the limit to which VDD can be lowered in Sleep mode, or during a device Reset, without losing RAM data.

- 2:** The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD

MCLR = VDD; WDT enabled/disabled as specified.

- 3:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR,...).

- 4:** For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2R_{EXT}$ (mA) with REXT in kΩ.

22.1 DC Characteristics: PIC18FXX2 (Industrial, Extended) PIC18LFXX2 (Industrial) (Continued)

PIC18LFXX2 (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial					
PIC18FXX2 (Industrial, Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended					
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
D010A	I _{DD}	Supply Current^(2,4)					
		PIC18LFXX2	—	14	30	μA	LP osc, F _{OSC} = 32 kHz, WDT disabled V _{DD} = 2.0V, -40°C to $+85^{\circ}\text{C}$
D010A		PIC18FXX2	—	60	150	μA	LP osc, F _{OSC} = 32 kHz, WDT disabled V _{DD} = 4.2V, -40°C to $+85^{\circ}\text{C}$
			—	60	180	μA	V _{DD} = 4.2V, -40°C to $+125^{\circ}\text{C}$
D022A	ΔI _{BOR}	Module Differential Current					
		Brown-out Reset PIC18LFXX2	—	29	40	μA	V _{DD} = 2.0V, $+25^{\circ}\text{C}$
			—	29	45	μA	V _{DD} = 2.0V, -40°C to $+85^{\circ}\text{C}$
D022A		Brown-out Reset PIC18FXX2	—	33	50	μA	V _{DD} = 4.2V, -40°C to $+85^{\circ}\text{C}$
			—	36	45	μA	V _{DD} = 4.2V, $+25^{\circ}\text{C}$
D022A		PIC18FXX2	—	36	50	μA	V _{DD} = 4.2V, -40°C to $+85^{\circ}\text{C}$
			—	36	65	μA	V _{DD} = 4.2V, -40°C to $+125^{\circ}\text{C}$
D022B	ΔI _{LVD}	Low-Voltage Detect PIC18LFXX2	—	29	40	μA	V _{DD} = 2.0V, $+25^{\circ}\text{C}$
			—	29	45	μA	V _{DD} = 2.0V, -40°C to $+85^{\circ}\text{C}$
		—	33	50	μA	V _{DD} = 4.2V, -40°C to $+85^{\circ}\text{C}$	
D022B		Low-Voltage Detect PIC18FXX2	—	33	45	μA	V _{DD} = 4.2V, $+25^{\circ}\text{C}$
			—	33	50	μA	V _{DD} = 4.2V, -40°C to $+85^{\circ}\text{C}$
		—	33	65	μA	V _{DD} = 4.2V, -40°C to $+125^{\circ}\text{C}$	

Legend: Shading of rows is to assist in readability of the table.

Note 1: This is the limit to which V_{DD} can be lowered in Sleep mode, or during a device Reset, without losing RAM data.

- 2:** The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all I_{DD} measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD}

MCLR = V_{DD}; WDT enabled/disabled as specified.

- 3:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{DD} or V_{SS} and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR,...).
- 4:** For RC osc configuration, current through R_{EXT} is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in kΩ.

PIC18FXX2

2. Module: Low-Voltage Detect Characteristics

Some of the values for parameter D420 in Table 22-1 of the Device Data Sheet have been updated (modified text is shown in **bold**).

TABLE 22-1: LOW-VOLTAGE DETECT CHARACTERISTICS

				Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param No.	Symbol	Characteristic		Min	Typ	Max	Units	Conditions
D420	VLVD	LVD Voltage on VDD transition high-to-low	LVV = 0001	1.96	2.06	2.16	V	$T \geq 25^{\circ}\text{C}$
			LVV = 0010	2.16	2.27	2.38	V	$T \geq 25^{\circ}\text{C}$
			LVV = 0011	2.35	2.47	2.59	V	$T \geq 25^{\circ}\text{C}$
			LVV = 0100	2.43	2.56	2.69	V	
			LVV = 0101	2.64	2.78	2.92	V	
			LVV = 0110	2.75	2.89	3.03	V	
			LVV = 0111	2.95	3.1	3.26	V	
			LVV = 1000	3.24	3.41	3.58	V	
			LVV = 1001	3.43	3.61	3.79	V	
			LVV = 1010	3.53	3.72	3.91	V	
			LVV = 1011	3.72	3.92	4.12	V	
			LVV = 1100	3.92	4.13	4.34	V	
			LVV = 1101	4.11	4.33	4.55	V	
			LVV = 1110	4.41	4.64	4.87	V	

3. Module: Packaging (Pinout and Product Identification)

PIC18F442 and PICF452 devices are now offered in 44-pin, near chip scale micro lead frame packages (commonly known as “QFN”). This packaging type has been added to the product line since the latest revision of the Device Data Sheet.

The addition of this option requires the following additions to the Device Data Sheet (DS39564B). The referenced figures and tables follow this text.

1. The “Pin Diagrams” on pages 2-3 of the Data Sheet are amended with the addition of the 44-pin QFN pinout, shown in Figure 1.
2. Table 1-3 of **Section 1.0 “Device Overview”** is replaced with an updated version which adds a column for QFN pin assignments. A row is also added for previously unlisted NC pins. All new information is indicated in **bold**.

3. **Section 24.1 “Package Marking Information”** is amended to include a marking template and example for 44-pin QFN devices. These are shown in Figure 2.

4. **Section 24.2 “Package Details”** is amended to include the mechanical drawing of the 44-pin QFN package, shown in Figure 3.

5. In the **“PIC18FXX2 Product Identification System”** (page 329), the “Package” options are amended to include the new line item:
ML = QFN

6. For the sake of completeness, it is also noted that the package designation “MLF” is now replaced by “QFN” in all occurrences throughout the Device Data Sheet. “MLF” should be considered an obsolete term.

FIGURE 1: PINOUT DIAGRAM FOR PIC18F442/452, 44-PIN QFN PACKAGE

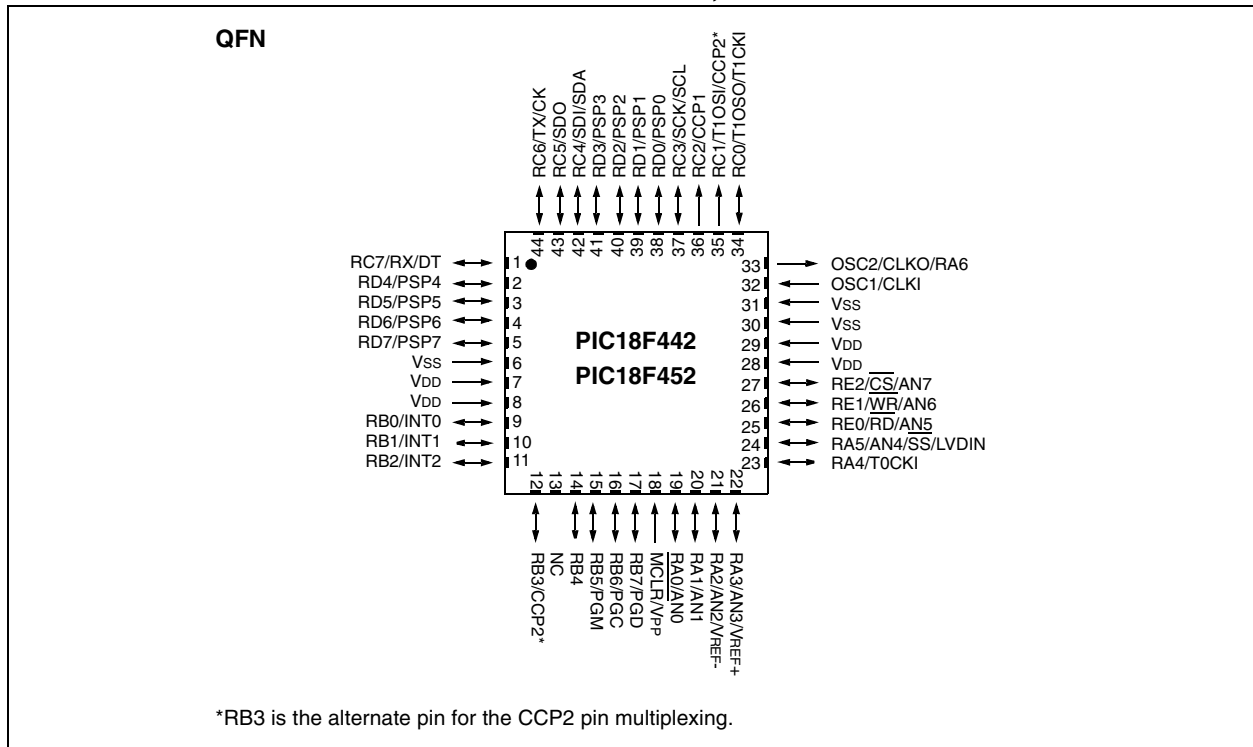
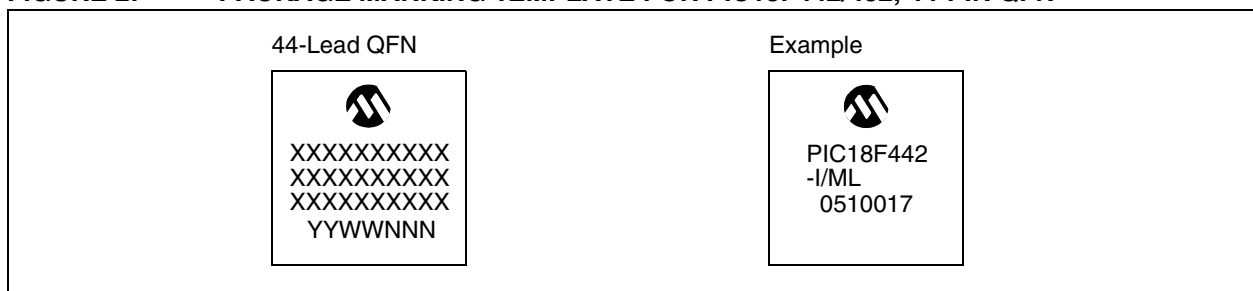


FIGURE 2: PACKAGE MARKING TEMPLATE FOR PIC18F442/452, 44-PIN QFN



PIC18FXX2

TABLE 1-3: PIC18F4X2 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	DIP	PLCC	QFN	TQFP			
MCLR/VPP MCLR VPP	1	2	18	18	I I	ST ST	Master Clear (input) or high-voltage ICSP™ programming enable pin. Master Clear (Reset) input. This pin is an active low Reset to the device. High-voltage ICSP programming enable pin.
NC	—		32		—	—	These pins should be left unconnected.
OSC1/CLKI OSC1 CLKI	13	14	33	30	I I	ST CMOS	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode, CMOS otherwise. External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.)
OSC2/CLKO/RA6 OSC2 CLKO RA6	14	15		31	O O I/O	— — TTL	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. General purpose I/O pin.
RA0/AN0 RA0 AN0 RA1/AN1 RA1 AN1 RA2/AN2/VREF- RA2 AN2 VREF- RA3/AN3/VREF+ RA3 AN3 VREF+ RA4/T0CKI RA4 T0CKI RA5/AN4/SS/LVDIN RA5 AN4 SS LVDIN RA6	2 3 4 5 6 7	3 4 5 6 8	19 20 21 22 23 24	19 20 21 22 23 24	I/O I I/O I I/O I I I/O I I/O I I I/O I I I	TTL Analog TTL Analog TTL Analog Analog TTL Analog Analog ST/OD ST TTL Analog ST Analog	PORTA is a bidirectional I/O port. Digital I/O. Analog input 0. Digital I/O. Analog input 1. Digital I/O. Analog input 2. A/D Reference Voltage (Low) input. Digital I/O. Analog input 3. A/D Reference Voltage (High) input. Digital I/O. Open-drain when configured as output. Timer0 external clock input. Digital I/O. Analog input 4. SPI™ Slave Select input. Low-Voltage Detect input. (See the OSC2/CLKO/RA6 pin.)

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
O = Output
OD = Open-Drain (no P diode to VDD)

CMOS = CMOS compatible input or output
I = Input
P = Power

TABLE 1-3: PIC18F4X2 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	DIP	PLCC	QFN	TQFP			
RB0/INT0 RB0 INT0	33	36	9	8	I/O I	TTL ST	PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs. Digital I/O. External Interrupt 0.
RB1/INT1 RB1 INT1	34	37	10	9	I/O I	TTL ST	Digital I/O. External Interrupt 1.
RB2/INT2 RB2 INT2	35	38	11	10	I/O I	TTL ST	Digital I/O. External Interrupt 2.
RB3/CCP2 RB3 CCP2	36	39	12	11	I/O I/O	TTL ST	Digital I/O. Capture2 input, Compare2 output, PWM2 output.
RB4	37	41	14	14	I/O	TTL	Digital I/O. Interrupt-on-change pin.
RB5/PGM RB5 PGM	38	42	15	15	I/O I/O	TTL ST	Digital I/O. Interrupt-on-change pin. Low-voltage ICSP™ programming enable pin.
RB6/PGC RB6 PGC	39	43	16	16	I/O I/O	TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming clock pin.
RB7/PGD RB7 PGD	40	44	17	17	I/O I/O	TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input
 ST = Schmitt Trigger input with CMOS levels
 O = Output
 OD = Open-Drain (no P diode to VDD)

CMOS = CMOS compatible input or output
 I = Input
 P = Power

PIC18FXX2

TABLE 1-3: PIC18F4X2 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	DIP	PLCC	QFN	TQFP			
RC0/T1OSO/T1CKI RC0 T1OSO T1CKI	15	16	34	32	I/O O I	ST — ST	PORTC is a bidirectional I/O port. Digital I/O. Timer1 oscillator output. Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2 RC1 T1OSI CCP2	16	18	35	35	I/O I I/O	ST CMOS ST	Digital I/O. Timer1 oscillator input. Capture2 input, Compare2 output, PWM2 output.
RC2/CCP1 RC2 CCP1	17	19	36	36	I/O I/O	ST ST	Digital I/O. Capture1 input/Compare1 output/ PWM1 output.
RC3/SCK/SCL RC3 SCK SCL	18	20	37	37	I/O I/O I/O	ST ST ST	Digital I/O. Synchronous serial clock input/output for SPI™ mode. Synchronous serial clock input/output for I ² C™ mode.
RC4/SDI/SDA RC4 SDI SDA	23	25	42	42	I/O I I/O	ST ST ST	Digital I/O. SPI Data In. I ² C Data I/O.
RC5/SDO RC5 SDO	24	26	43	43	I/O O	ST —	Digital I/O. SPI Data Out.
RC6/TX/CK RC6 TX CK	25	27	44	44	I/O O I/O	ST — ST	Digital I/O. USART Asynchronous Transmit. USART Synchronous Clock (see related RX/DT).
RC7/RX/DT RC7 RX DT	26	29	1	1	I/O I I/O	ST ST ST	Digital I/O. USART Asynchronous Receive. USART Synchronous Data (see related TX/CK).

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
O = Output
OD = Open-Drain (no P diode to VDD)

CMOS = CMOS compatible input or output
I = Input
P = Power

TABLE 1-3: PIC18F4X2 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	DIP	PLCC	QFN	TQFP			
RD0/PSP0	19	21	38	38	I/O	ST TTL	PORTD is a bidirectional I/O port, or a Parallel Slave Port (PSP) for interfacing to a microprocessor port. These pins have TTL input buffers when the PSP module is enabled. Digital I/O. Parallel Slave Port Data.
RD1/PSP1	20	22	39	39	I/O	ST TTL	Digital I/O. Parallel Slave Port Data.
RD2/PSP2	21	23	40	40	I/O	ST TTL	Digital I/O. Parallel Slave Port Data.
RD3/PSP3	22	24	41	41	I/O	ST TTL	Digital I/O. Parallel Slave Port Data.
RD4/PSP4	27	30	2	2	I/O	ST TTL	Digital I/O. Parallel Slave Port Data.
RD5/PSP5	28	31	3	3	I/O	ST TTL	Digital I/O. Parallel Slave Port Data.
RD6/PSP6	29	32	4	4	I/O	ST TTL	Digital I/O. Parallel Slave Port Data.
RD7/PSP7	30	33	5	5	I/O	ST TTL	Digital I/O. Parallel Slave Port Data.
RE0/ $\overline{\text{RD}}$ /AN5 RE0 $\overline{\text{RD}}$	8	9	25	25	I/O	ST TTL	PORTE is a bidirectional I/O port. Digital I/O. Read control for parallel slave port (see also $\overline{\text{WR}}$ and $\overline{\text{CS}}$ pins). Analog input 5.
AN5 RE1/ $\overline{\text{WR}}$ /AN6 RE1 $\overline{\text{WR}}$	9	10	26	26	I/O	ST TTL	Digital I/O. Write control for parallel slave port (see $\overline{\text{CS}}$ and $\overline{\text{RD}}$ pins). Analog input 6.
AN6 RE2/ $\overline{\text{CS}}$ /AN7 RE2 $\overline{\text{CS}}$	10	11	27	27	I/O	ST TTL	Digital I/O. Chip Select control for parallel slave port (see related $\overline{\text{RD}}$ and $\overline{\text{WR}}$). Analog input 7.
AN7						Analog	
Vss	12, 31	13, 34	6, 30, 31	6, 29	P	—	Ground reference for logic and I/O pins.
VDD	11, 32	12, 35	7, 8, 28, 29	7, 28	P	—	Positive supply for logic and I/O pins.
NC	—	1, 17, 28	13	12, 13, 33, 34	—	—	These pins are not internally connected. They should be left unconnected.

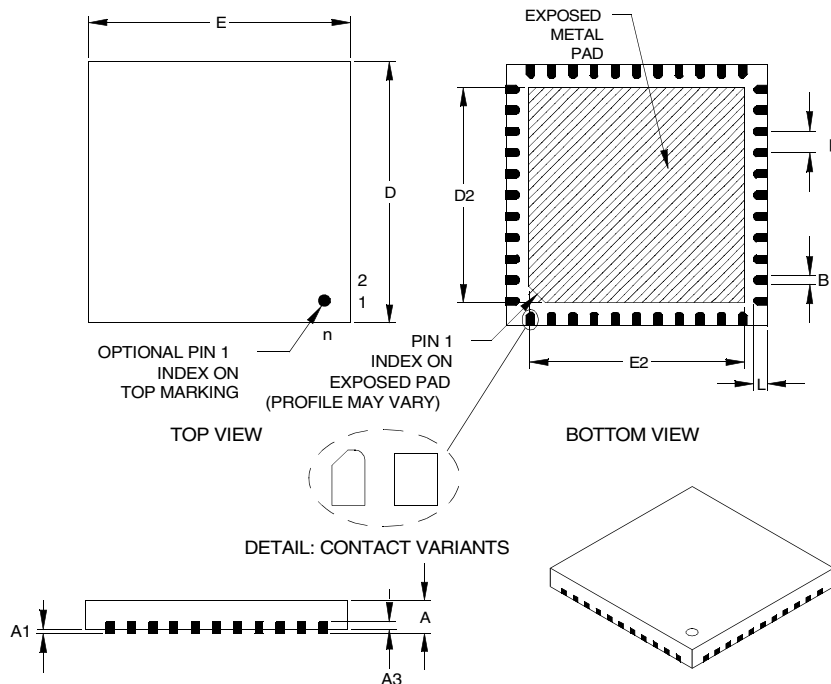
Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
O = Output
OD = Open-Drain (no P diode to VDD)

CMOS = CMOS compatible input or output
I = Input
P = Power

PIC18FXX2

FIGURE 3: 44-PIN QFN PACKAGE

44-Lead Plastic Quad Flat No Lead Package (ML) 8x8 mm Body (QFN)



Dimension Limits	Units	INCHES			MILLIMETERS*		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Contacts	n		44			44	
Pitch	P	.026 BSC ¹			0.65 BSC ¹		
Overall Height	A	.031	.035	.039	0.80	0.90	1.00
Standoff	A1	.000	.001	.002	0	0.02	0.05
Base Thickness	A3	.010 REF ²			0.25 REF ²		
Overall Width	E	.309	.315	.321	7.85	8.00	8.15
Exposed Pad Width	E2	.236	.258	.260	5.99	6.55	6.60
Overall Length	D	.309	.315	.321	7.85	8.00	8.15
Exposed Pad Length	D2	.236	.258	.260	5.99	6.55	6.60
Contact Width	B	.008	.013	.013	0.20	0.33	0.35
Contact Length	L	.014	.016	.019	0.35	0.40	0.48

*Controlling Parameter

Notes:

1. BSC: Basic Dimension. Theoretically exact value shown without tolerances.

See ASME Y14.5M

2. REF: Reference Dimension, usually without tolerance, for information purposes only.

See ASME Y14.5M

Exposed pad varies according to die attach paddle size.

JEDEC equivalent: M0-220

Drawing No. C04-103, Revised 05-05-05

REVISION HISTORY

Rev A Document (10/2003)

First revision of this document. Listed silicon issues 1 (Core – Program Memory Space), 2 (Data EEPROM), 3 and 4 (MSSP) and 5 (Core – Instruction Set) and data sheet clarification issues 1 (DC Characteristics), 2 (Low-Voltage Detect Characteristics) and 3 (Packaging – Pinout and Product Identification).

Rev B Document (05/2005)

Added silicon issue 6 (Reset).

Rev C Document (08/2005)

Moved silicon issue 4 (MSSP) to MSSP module errata and added silicon issue 6 (Program Memory).

PIC18FXX2

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KEELOQ, microID, MPLAB, PIC, PICmicro, PICSTART, PRO MATE, PowerSmart, rPIC, and SmartShunt are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.


AmpLab, FilterLab, Migratable Memory, MXDEV, MXLAB, PICMASTER, SEEVAL, SmartSensor and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, dsPICDEM, dsPICDEM.net, dsPICworks, ECAN, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, Linear Active Thermistor, MPASM, MPLIB, MPLINK, MPSIM, PICkit, PICDEM, PICDEM.net, PICLAB, PICtail, PowerCal, PowerInfo, PowerMate, PowerTool, rLAB, rPICDEM, Select Mode, Smart Serial, SmartTel, Total Endurance and WiperLock are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2005, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949:2002 ==

Microchip received ISO/TS-16949:2002 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona and Mountain View, California in October 2003. The Company's quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.



WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://support.microchip.com>
Web Address:
www.microchip.com

Atlanta

Alpharetta, GA
Tel: 770-640-0034
Fax: 770-640-0307

Boston

Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago

Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas

Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit

Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo

Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles

Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

San Jose

Mountain View, CA
Tel: 650-215-1444
Fax: 650-961-0286

Toronto

Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Australia - Sydney

Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing

Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu

Tel: 86-28-8676-6200
Fax: 86-28-8676-6599

China - Fuzhou

Tel: 86-591-8750-3506
Fax: 86-591-8750-3521

China - Hong Kong SAR

Tel: 852-2401-1200
Fax: 852-2401-3431

China - Qingdao

Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai

Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang

Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen

Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Shunde

Tel: 86-757-2839-5507
Fax: 86-757-2839-5571

China - Wuhan

Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian

Tel: 86-29-8833-7250
Fax: 86-29-8833-7256

ASIA/PACIFIC

India - Bangalore

Tel: 91-80-2229-0061
Fax: 91-80-2229-0062

India - New Delhi

Tel: 91-11-5160-8631
Fax: 91-11-5160-8632

India - Pune

Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama

Tel: 81-45-471-6166
Fax: 81-45-471-6122

Korea - Gumi

Tel: 82-54-473-4301
Fax: 82-54-473-4302

Korea - Seoul

Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Penang

Tel: 604-646-8870
Fax: 604-646-5086

Philippines - Manila

Tel: 632-634-9065
Fax: 632-634-9069

Singapore

Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu

Tel: 886-3-572-9526
Fax: 886-3-572-6459

Taiwan - Kaohsiung

Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei

Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok

Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Weis

Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark - Copenhagen

Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris

Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich

Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan

Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen

Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid

Tel: 34-91-352-30-52
Fax: 34-91-352-11-47

UK - Wokingham

Tel: 44-118-921-5869
Fax: 44-118-921-5820