MM912_634, Silicon Analog Mask (M91W) / Digital Mask (N53A) Errata

This errata document applies to the MM912_634 product family.

Table 1. Orderable Part Number Identification

Part Number	Analog Mass ID	Analog Pass	MCU Mask ID	Package
MM912G634CM1AE	DA05M91W	2.4	DA00N53A	48 LQFP-EP
MM912G634CV1AE				
MM912H634CM1AE				
MM912H634CV1AE				
MM912G634CV2AP				48 LQFP
MM912G634DM1AE	DA06M91W	2.5		48 LQFP-EP
MM912G634DV1AE				
MM912H634DM1AE				
MM912H634DV1AE				
MM912G634DV2AP				48 LQFP

1 Device Revision Identification

The device revision is indicated by a 1-character code after the device code. For instance the “C” in the “MM912H634CV1AE” indicates revision 2.4. All standard devices are marked with a device identification and build information code.

2 Device Build Information / Date Code

The marked trace code is the link between the physically marked materials and the manufacturing lot’s system genealogy information. Once the connection between the marked material and system genealogy information is made, traceability reports provide the material’s manufacturing/shipping history. All devices listed in the Errata are affected unless specific date codes are provided below.

3 Description

The following table provides the general definitions of the errata severity in this document.

Table 2. Definitions of Errata Severity

Errata Severity Level	Meaning
High	Failure mode that severely inhibits the use of the device for all or a majority of intended applications
Medium	Failure mode that might restrict or limit the use of the device for all or a majority of intended applications
Low	Unexpected behavior that does not cause significant problems for the intended applications of the device
Enhancement	Improvement made to the device due to previously found issues on the design

3.0.1 Silicon Revision Register - SRR

The analog die contains a silicon revision register to read the actual revision information.

- Mask M91W-F corresponds to silicon revision 2.4;
- Mask M91W-G corresponds to silicon revision 2.5;

The actual revision of the analog die is available in the SRR (Silicon Revision Register), accessible through the Die-to-Die interface.

Register Details

Offset [1] 0xF4 Access: Read only

		7	6	5	4	3	2	1	0
R		0	0	0	0	FMREV		MMREV	
W									
Default Values	M91W-F	0	0	0	0	0	1	1	0
	M91W-G	0	0	0	0	1	1	0	0

Notes

1. Offset related to 0x0200 for blocking access and 0x300 for non blocking access, within the global address space.

Field	Description
3-2 FMREV	MM912_634 analog die Silicon Revision Register - These bits represent the revision of Silicon of the analog die. They are incremented for every full mask or metal mask issued of the device. One number is set for one revision of the silicon of the analog die.
1-0 MMREV	

Note:

All the following errata items are valid for all silicon revisions unless explicitly stated.

Multiple Readings of the ADC Bandgap Channel

Severity Level – High

Description of Problem

Multiple (>4) consecutive conversions of Channel 14 causes the Low-side drivers to turn off.

The Channel 14 conversion samples the independent internal bandgap reference (bg1p25sleep). Charging the sample capacitor results in an unintended decrease in the reference voltage. Because the reference voltage determines the value of the VREG high voltage detection threshold, the decrease in the reference voltage causes a corresponding decrease in the high voltage threshold. This activates the VREG-HV mechanism for low-side shutdown even thought the actual voltage regulator output may be within normal operating range. (See section 5.13 “Low-side Drivers - LSx” in the datasheett MM912_634D1.)

Customer Impact or Symptoms

Low-side drivers are turned off.

Workaround

Customers must not perform continuous conversions on channel 14. The number of consecutive channel 14 readings must not exceed four readings within a 400 µs cycle.

Low-side Control Enable (LSCEN) Register not resetting on VREG Over-voltage Condition

Severity Level – Low

Description of Problem

The Low-side Control Enable (LSCEN) register is reset only after LVR, LVRX and POR. It does not reset in case of an VREG Over-voltage event. See Figure 1. Low-side Block Diagram.

A digital implementation issue prevents the LSCEN register from resetting when a VREG high voltage condition occurs. The intent of the LSCEN register is to create a secondary deactivation stage for the low-side drivers, thereby verifying that the VDD-Digital and the Sleep2p5 Digital circuitry is functional after the occurrence of a VREG high voltage condition.

LS drivers shutdowns can be implemented via the VREG OVER-VOLTAGE FLAG, which then must be acknowledged by software (IRQ optional).

In spite of the design issue, the basic intent of the feature remains valid because functional VDD-Digital and the Sleep2p5 Digital circuitry is still required for the LS to be active. Other than the exception indicated above, the register continues to perform as specified. (That is, it does not reset when a high voltage condition occurs and therefore would not need to be written to in order to reactivate the low-side drivers.)

Customer Impact or Symptoms

The Low-side Control Enable (LSCEN) register does not reset after a VREG Over-voltage event.

Workaround

To maintain compatibility with a potential future silicon fix, Freescale recommends using the register write LSCEN=0x5 to re-enable the low-side.

The above restrictions notwithstanding, the intended security function of the feature remains in place.

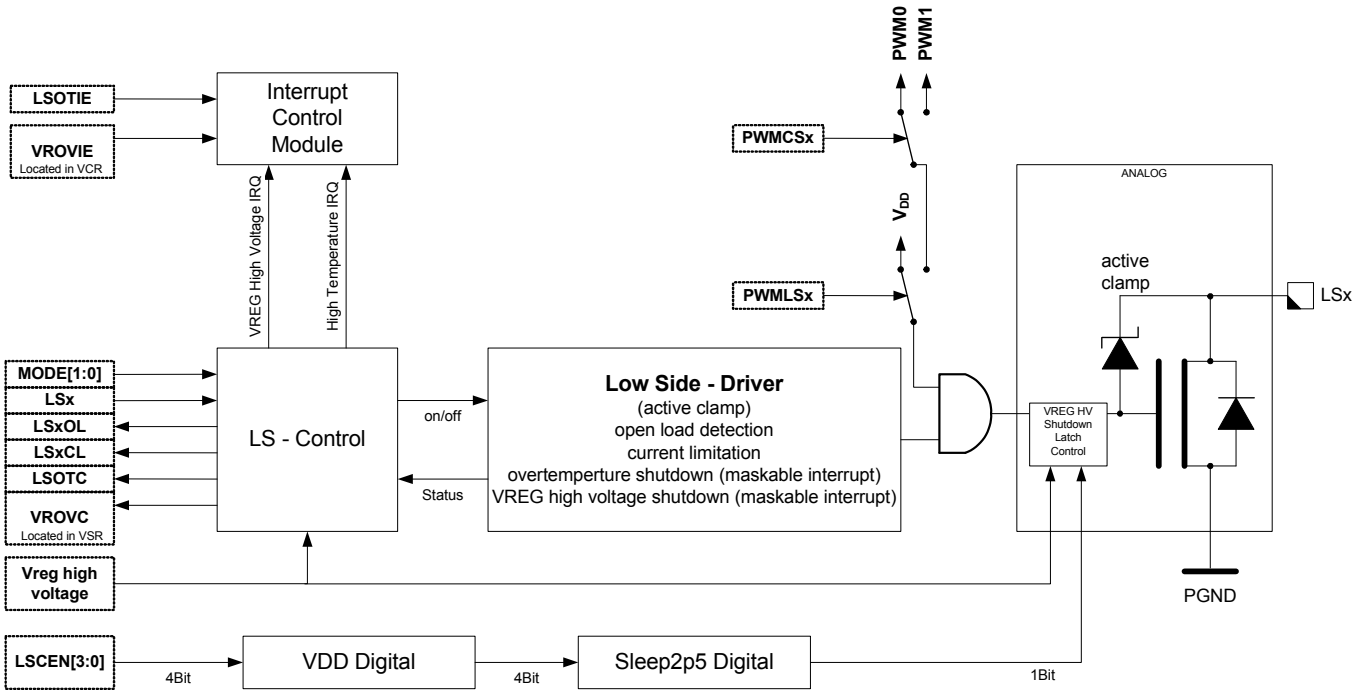

Figure 1. Low-side Block Diagram

AD Converter Not Functional with ADC Clock Equal to D2D Clock

Severity Level – Low

Description of Problem

The ADC does not operate correctly with the ADCCLK = D2DCLK (Prescaler = 1).

With the current implementation of the ADC state machine, the D2DCLK frequency must be higher than the ADCCLK frequency in order for the ADC to perform to specification. The ADC does not operate correctly when ADCCLK frequency and the D2DCLK frequency are equal. Because the ADCCLK frequency must be in the range specified as fADC (typ. 2.0 MHz), this problem only occurs when D2DCLK frequencies are in the same range.

Customer Impact or Symptoms

The ADC does not function properly.

Workaround

The setting of the ADC Clock Prescaler = 1 (PS[2:0]=101, 110 or 111) must not be used when performing ADC measurements.

Multiple Resets On Power Down With Large VSUP Capacitor Values

Severity Level – Medium

Description of Problem

With a large value of VSUP (>100 µF) during power down, the RST/RESET_A line may toggle multiple times, causing the microcontroller to execute power-on resets.

The MM912_634 has several regulators used for internal functions that are not mentioned in the datasheet. One of the 2.5 V regulators, “sleep2p5”, is used to power the sleep mode features of the device during sleep mode when the normal mode VDD regulator is shut down. This regulator has an associated low voltage reset signal (LVR) that is activated at 1.8 V (power down) and released at 2.2 V (power up).

The sequence of events at power down is as follows:

1. VSUP begins to decay. When VSUP goes below (2.5 V + sleep2p5 headroom), the sleep2p5 output voltage begins to decay.
2. When sleep2p5 voltage reaches 1.8 V, its LVR goes low.
3. When the LVR goes low, a number of internal modules normally powered by 2sleep5 are disabled, reducing the load on the sleep2p5 regulator.
4. This reduced load reduces the value of sleep2p5 headroom, causing its output voltage to increase.
5. If the sleep2p5 output voltage increases above 2.2 V, the LVR is released, causing the internal modules to reactivate and the microcontroller to execute a power on reset (POR).
6. With a sufficiently large VSUP capacitor, the slow decay of VSUP can cause multiple PORs as described above.

Customer Impact or Symptoms

The microcontroller executes resets during a power down.

Workaround

If possible in the application, the value of the VSUP capacitor should be decreased to increase the decay rate of VSUP during power down. A value of 47 µF or less is recommended. If this is not possible, a software delay of at least 1.0 ms should be included before any code is executed following a power-on-reset.

Stop Mode Wake-Up generating Reset and rising WUR bit into RSR register

Severity Level – Medium

Description of Problem

After a transition from Stop mode to Normal mode due to a wake-up event, the device may generate a Reset. If this occurs, the WUR bit in the RSR register is set until a reading of RSR register occurs. This behavior will affect parts with VDD in Stop mode below LVR in Normal mode.

When a wake-up event occurs, the transition from stop mode to normal mode begins. The VDD stop regulator switches to VDD normal regulator. The LVR normal mode is activated. If the actual VDD regulator output voltage is below LVR normal, the device generates a reset on the RESETA pin.

When an LVR condition occurs on VDD during a transition from Low Power to Normal, a RESET is performed and the WUR bit is set into RSR register. This is the standard behavior during wake-up from Sleep mode.

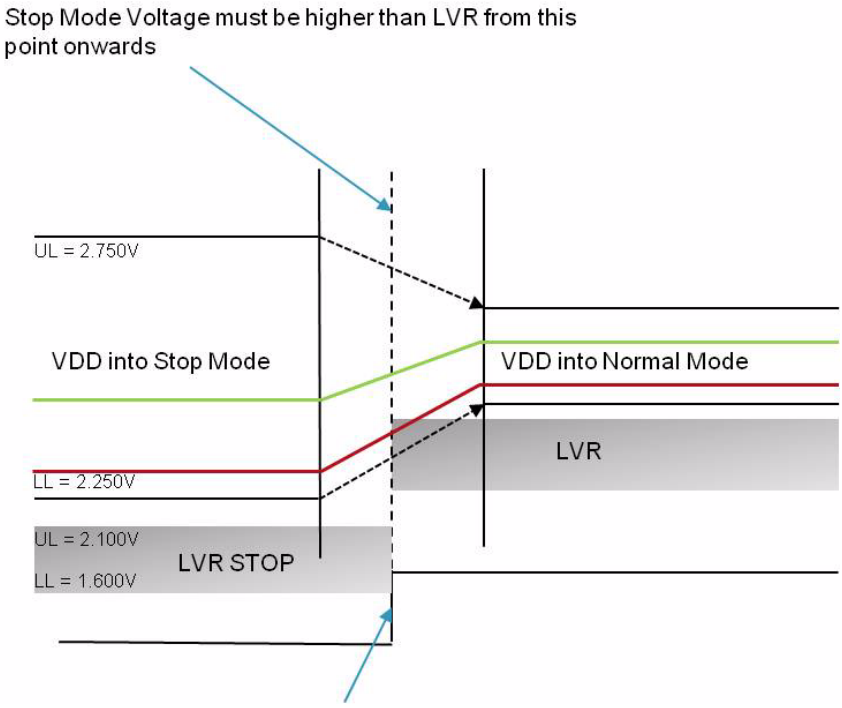

Figure 2. Stop mode to Normal mode Transition

In **Figure 2**, the green line denotes a part that does not show this behavior. The red lines denotes a part that does show this behavior. The VDD parameter in Stop mode is distributed between 2.25 V and 2.75 V, while the LVR Normal is max 2.40 V. Only devices that have an actual VDD stop between 2.25 V and 2.40 V will exhibit this behavior.

Customer Impact or Symptoms

A RESET is performed and the WUR bit is set into the RSR register during a wakeup from Stop Mode.

Workaround

There is no workaround possible to prevent the occurrence of this behavior.
The software recommendation to help minimize the impact of the behavior consists of verifying the Reset source after a wake-up. This check might be performed after a return from the reset sequence. If a reset occurs, the following flag is as described below:

1. WUR bit is set to 1 into RSR register, indicating a Wake-Up reset.

2.PORF bit is set to 0 into CPMUFLG register indicating:

a) VDDRX, MCU supply, did not cross the Power-On-Reset threshold (PORF will be set to 1 in the case of wake-up from Sleep mode).

b) VDDRX and VDDX remain unchanged and are still inside their operating conditions.

The wake-up source can be identified from the Wake-up Source Register (WSR).

The RAM content will not be altered by this behavior as VDDRX remains in operating conditions during this transition. The program will start from its beginning following the reset sequence.

Notice that the RAM cannot be accessed between MCU wake-up and reset generation. The delay for the MCU to start executing its code is longer than the delay for the analog to generate the reset.

Note:

Freescale recommends that you use only the VDD output to supply the VDD2D input and that you avoid any additional current load.

Fix Plan

Errata applies to the “C” version of silicon:
MM912G634CM1AE
MM912G634CV1AE
MM912H634CM1AE
MM912H634CV1AE
MM912G634CV2AP

Errata corrected on the “D” version of silicon:
MM912G634DV2AP
MM912G634DM1AE
MM912G634DV1AE
MM912H634DM1AE
MM912H634DV1AE

Unexpected setting of VROVC Bit and disabling of Low-side Driver(s) at V_{SUP} Power On

Severity Level – Medium

Description of the Problem:

During certain dynamic voltage start-up conditions (V_{BATT} cranking condition, slow V_{BATT} ramp up, etc.), multiple assertions and de-assertions of the V_{DD} and V_{DDX} regulators cause multiple resets from the MCU to be sent to the analog driver. This causes the desired Sleep Band Gap trim value CTR2 (set by the user) to be replaced with the default value (-12%). This in turn causes the trimmed Sleep Band Gap (SLPBGP) voltage to be set too low. Consequently, a voltage regulator overvoltage condition (VROVC) fault is triggered and the bit set to 1 in the Voltage Status register (VSR). Subsequently, the low-side drivers are disabled (see chapter 5.13.4.1 Voltage Regulator Overvoltage protection in the 5.13 Low-side drivers Section of the data sheet).

Due to a clock synchronization condition which can be encountered during a multiple reset event, the proper CTR2 trim loaded by a user can be replaced by the default CTR2 trim value. This default trim value then becomes loaded and locked into the analog trim register block of the analog driver.

Because the default CTR2 trim value (-12%) is locked in the analog trim register block, no other CTR2 trim parameter can be loaded by the user without first completing a device power-down.

The contents loaded into the analog trim register block cannot be read back directly by the user. The user only has read access to the contents of digital CTR2 trim register block, whose contents are clocked into the analog trim register block.

As a consequence, if after last reset event the user executes software to re-load the proper trim word, the new value is reflected in the digital CTR2 register. However, this value is NOT loaded into the analog trim register, and the VROVC reset condition remains set.

4.25.1.2.3 Trimming Register 2 (CTR2)

Table 208. Trimming Register 2 (CTR2)

Offset[149] 0xF2 — Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	SLPBGTRE	SLPBG_LOCK	SLPBGTR2	SLPBGTR1	SLPBGTR0
W								
Reset	0	0	0	0	0	0	0	0

Note:
149. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Figure 3. Trimming Register 2

Customer Impact or Symptoms:

Following an unexpected POR or voltage transient on V_{SUP}, the VROVC bit is set to 1 and the low-side drivers are disabled. The VROVC bit can subsequently be cleared **only** with a full power-down of the device.

Workaround: Disable use of the SLPBGTRE_Lock Bit

By factory default, the SLPBGTR lock bit is set to 1 in the MCU IFR. The customer can disable use of the lock bit by masking this bit when loading the contents from the IFR into the analog die CTR2 register. Since this trim data is no longer locked, it does mean the contents of CTR2 digital register must be re-loaded by the user after each RESET event.

Of all the TRIM registers used in the device, only the CTR2 TRIM register has this locking feature. Therefore, disabling the use of this lock feature does not represent an unusual condition in which to operate the device.

4 Revision History

Revision	Date	Description of Changes
7.0	4/2015	• Added Revision History • Added - Unexpected setting of VROVC Bit and disabling of Low-side Driver(s) at Vsup Power On • Re-formatted document to conform to new Errata template

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