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November 2013

# FQD4P40

# P-Channel QFET® MOSFET

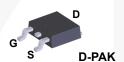
-400 V, -2.7 A, 3.1 Ω

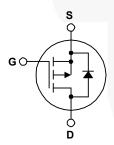
## **Description**

These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for electronic lamp ballast based on complimentary half bridge.

### **Features**

- -2.7 A, -400 V, R<sub>DS(on)</sub> = 3.1  $\Omega$  (Max.) @ V<sub>GS</sub> = -10 V, I<sub>D</sub> = -1.35 A
- Low Gate Charge (Typ. 18 nC)
- Low Crss (Typ. 11 pF)
- · 100% Avalanche Tested





## Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter		FQD4P40TM	Unit
$V_{DSS}$	Drain-Source Voltage		-400	V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C)		-2.7	Α
	- Continuous (T <sub>C</sub> = 100°C)		-1.71	Α
I <sub>DM</sub>	Drain Current - Pulsed	(Note 1)	-10.8	Α
V <sub>GSS</sub>	Gate-Source Voltage		± 30	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)		260	mJ
I <sub>AR</sub>	Avalanche Current	(Note 1)	-2.7	Α
E <sub>AR</sub>	Repetitive Avalanche Energy	(Note 1)	5.0	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		-4.5	V/ns
P <sub>D</sub>	Power Dissipation (T <sub>A</sub> = 25°C) *		2.5	W
	Power Dissipation (T <sub>C</sub> = 25°C) - Derate above 25°C		50	W
			0.4	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150	°C
T <sub>L</sub>	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

## **Thermal Characteristics**

Symbol	Parameter	FQD4P40TM	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	2.5	
В	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	110	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (*1 in <sup>2</sup> Pad of 2-oz Copper), Max.	50	

# **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQD4P40TM	FQD4P40	DPAK	Tape and Reel	330 mm	16 mm	2500 units

# **Electrical Characteristics** T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Off Cha	aracteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-400			V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = -250 μA, Referenced to 25°C		0.36		V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -400 V, V <sub>GS</sub> = 0 V			-1	μΑ
		V <sub>DS</sub> = -320 V, T <sub>C</sub> = 125°C			-10	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V			-100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V			100	nA
On Cha	racteristics					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$	-3.0		-5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -1.35 A		2.44	3.1	Ω
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = -50 \text{ V}, I_{D} = -1.35 \text{ A}$		2.5		S
	ic Characteristics				1	
C <sub>iss</sub>	Input Capacitance	$V_{DS} = -25 \text{ V}, V_{GS} = 0 \text{ V},$		520	680	pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz		80	105	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			11	15	pF
Switchi	ing Characteristics					
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = -200 V, I <sub>D</sub> = -3.5 A,		13	35	ns
t <sub>r</sub>	Turn-On Rise Time	$R_{G} = 25 \Omega$		55	120	ns
$t_{d(off)}$	Turn-Off Delay Time			35	80	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)		37	85	ns
Qg	Total Gate Charge	V <sub>DS</sub> = -320 V, I <sub>D</sub> = -3.5 A,		18	23	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = -10 V	/	3.8		nC
$Q_{gd}$	Gate-Drain Charge	(Note 4)		9.4		nC
	5. 1.01					
	Source Diode Characteristics at				-2.7	A
l <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current  Maximum Pulsed Drain-Source Diode Forward Current				-10.8	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -2.7 A			-5.0	V
t <sub>rr</sub>	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_S = -3.5 \text{ A},$		260	-5.0	ns
Q <sub>rr</sub>	Reverse Recovery Charge	$dl_{\rm F}$ / dt = 100 A/ $\mu$ s		1.4		μC
<b>∽</b> rr	Neverse Necovery Charge	αιρ / αι 100 / υμο		1.4		μ

#### Notes:

- Notes. 1. Repetitive rating: pulse-width limited by maximum junction temperature. 2. L = 62 mH,  $I_{AS}$  = -2.7 A,  $V_{DD}$  = -50 V,  $R_{G}$  = 25  $\Omega$ , starting  $T_{J}$  = 25°C. 3.  $I_{SD}$  ≤ -3.5 A, di/dt ≤ 200 A/ $\mu$ s,  $V_{DD}$  ≤ BV $_{DSS}$ , starting  $T_{J}$  = 25°C. 4. Essentially independent of operating temperature.

# **Typical Characteristics**

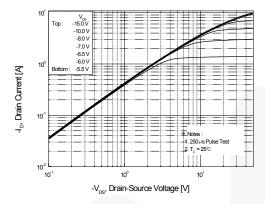


Figure 1. On-Region Characteristics

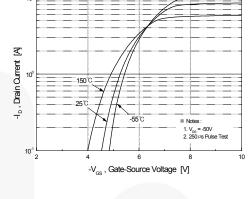


Figure 2. Transfer Characteristics

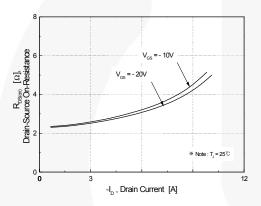


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

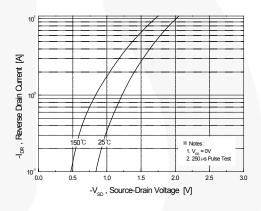


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

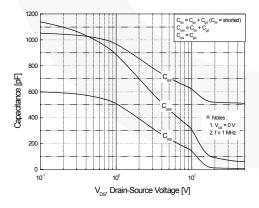


Figure 5. Capacitance Characteristics

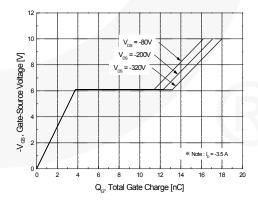


Figure 6. Gate Charge Characteristics

# Typical Characteristics (Continued)

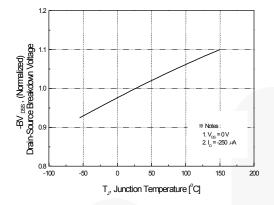


Figure 7. Breakdown Voltage Variation vs. Temperature

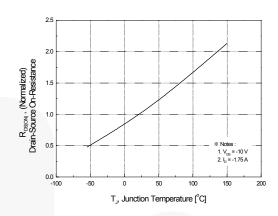


Figure 8. On-Resistance Variation vs. Temperature

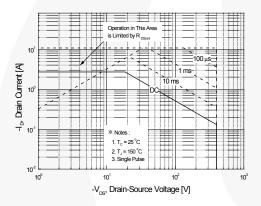


Figure 9. Maximum Safe Operating Area

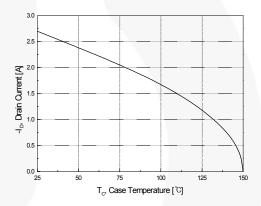


Figure 10. Maximum Drain Current vs. Case Temperature

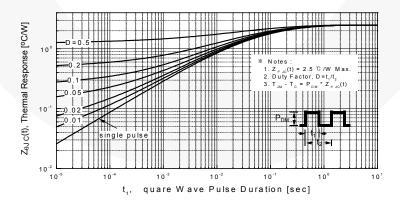


Figure 11. Transient Thermal Response Curve

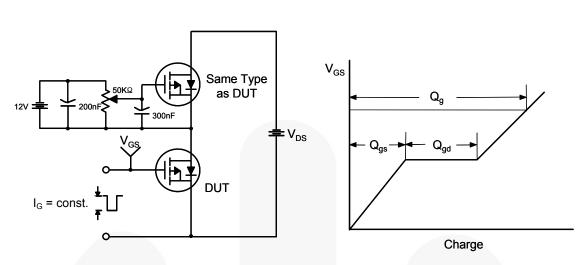


Figure 12. Gate Charge Test Circuit & Waveform

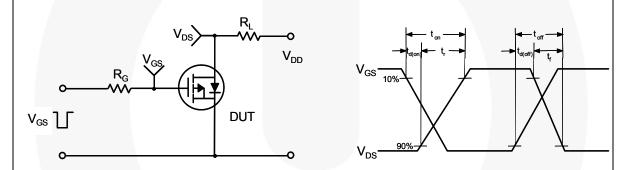


Figure 13. Resistive Switching Test Circuit & Waveforms

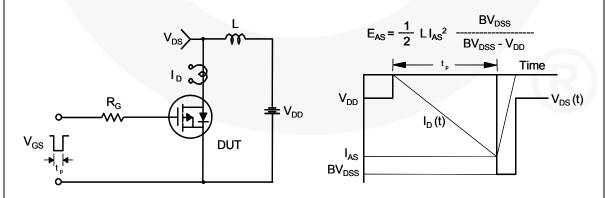
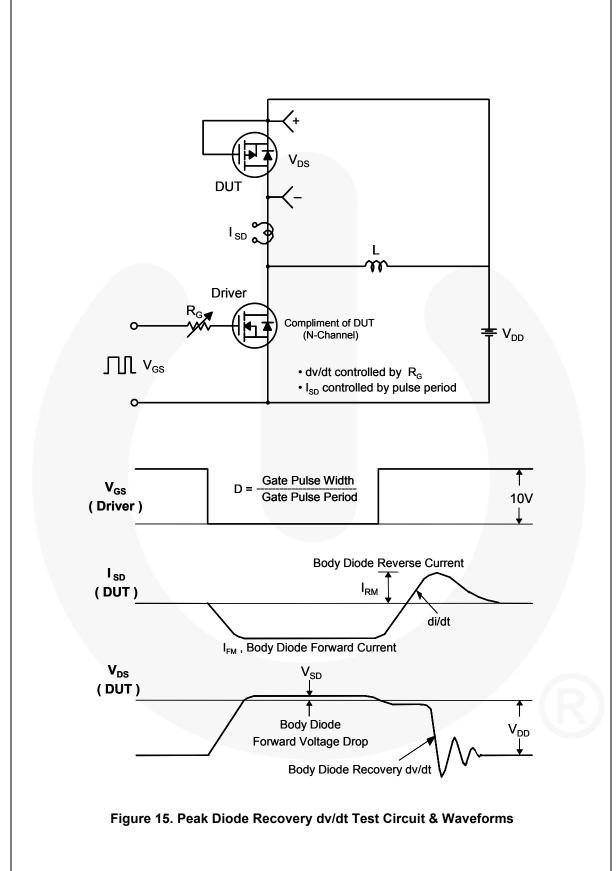


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



## **Mechanical Dimensions**

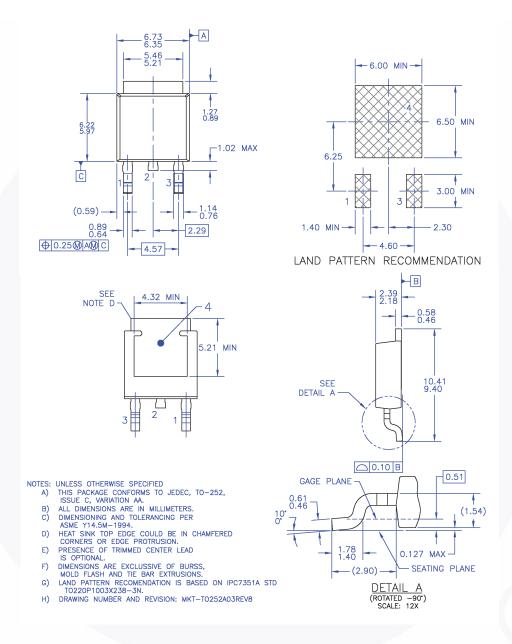


Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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